



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,202	09/24/2001	Hiroshi Takeno	P107242-00024	6219

7590

09/10/2003

Arent Fox Kintner Plotkin & Kahn  
Suite 600  
1050 Connecticut Avenue NW  
Washington, DC 20036-5339

EXAMINER

ANDERSON, MATTHEW A

ART UNIT

PAPER NUMBER

1765

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/926,202

Applicant(s)

TAKENO, HIROSHI

Examiner

Matthew A. Anderson

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 6-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wijaranakula (5,611,855) in view of Wolf et al. (Silicon Processing for the VLSI Era Volume 1: Process Technology, Lattice Press, Sunset Beach, CA, USA, pp. 26-30, 59-61, 124, 133-136).

Wijaranakula discloses a method of making an epitaxial Si wafer with certain properties. The process is disclosed in col. 4 lines 15+. A doped (with boron, arsenic, antimony) Si substrate with a dissolved oxygen concentration of between 10-50 ppma (parts per million atoms) is used. Col. 5 lines 1-67 details the growth of an epitaxial layer on the wafer. The Si epitaxial wafer is annealed at between 600°C and 900°C to form oxygen microdefects in the wafer.

Wijaranakula does not disclose the deposition temperature of the epitaxial layer or the oxygen concentration in units of atoms/cm<sup>3</sup>.

Wolf et al. discloses known Si physical properties. On page 59, the typical concentration of oxygen in Si is given as  $5 \times 10^{17}$  to  $1 \times 10^{18}$  atoms/cm<sup>3</sup> or 10-20 ppma. On page 135 it is disclosed that Si epitaxial growth is favored over etching in the range of temperatures from 900°C to 1400°C. Temperature optimization for annealing is disclosed on pages 60-61 and annealing from 650° to 750° C is discussed. On page 27 it is disclosed that Si doped with boron and antimony can have resistivities of from 0.005 ohm-cm upwards. Wolf et al. discloses the use of oxygen precipitates and denuded zones as gettering on page 61.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine Wijaranakula with Wolf et al. because Wolf discloses temperatures for epitaxial growth and annealing, a basis for comparing oxygen concentrations quoted in different units, resistivity of boron and antimony doped Si, and the known useful gettering action of oxygen precipitates in Si wafers.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to form a Si epitaxial wafer doped with boron (or antimony or arsenic) at a temperature of 1000°C or higher on a Si substrate having a oxygen concentration of  $4 \times 10^{17}$  to  $10 \times 10^{17}$  (equivalent to  $1 \times 10^{18}$ )/cm<sup>3</sup> and then heat treating the wafer at a temperature of from 450°C to 750°C because such is suggested by Wijaranakula in light of Wolf et al.

It would have been obvious to one of ordinary skill in the art at the time of the present invention that the resistivity of such a wafer would include the range of 0.02 ohm-cm or lower because such is disclosed by Wolf et al. for doped Si wafers and such

Art Unit: 1765

resistivity was disclosed by Wolf et al. on page 26 as known to be a function of doping concentration.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the process parameters including temperature such that oxygen precipitation nuclei were formed (thus increasing the bulk defect density) and not reducing the needed and well known use of the bulk Si oxygen precipitates for gettering purposes because Wolf et al. discloses such use for oxygen precipitates in the bulk of Si wafers and temperatures for annealing such wafers.

### ***Response to Arguments***

3. Applicant's arguments filed 6/20/2003 have been fully considered but they are not persuasive.

In response to the argument on page 5 of paper 14 that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The examiner has shown that the ranges and known results of the use of those ranges in oxygen precipitate gettered Si-epitaxial wafers typical in the art suggest the claimed Si epitaxial wafer.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The combined references described previously by the examiner suggest a silicon wafer with a grown epitaxial Si layer thereon which is subsequently annealed to produce oxygen precipitates (bulk defects therein) which were known to act as gettering sites. The oxygen concentrations and the temperatures claimed were within the known ranges described by the references. One of ordinary skill in the art would have expected gettering to occur in Si-epitaxial wafers grown under these conditions.

The claim that the gettering effect with a doped Si wafer is not suggested by the references is not persuasive. Wijaranakula discloses using a boron (i.e. a P-type) ,phosphorous (N-type), or non-doped (I-type) wafer in col. 4 lines 15-25. This, combined with Wolf et al. suggests the claimed gettered epitaxial –Si wafer manufacturing process.

### ***Conclusion***

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

Art Unit: 1765

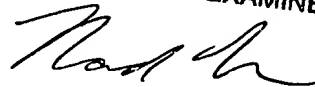
mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Anderson whose telephone number is (703) 308-0086. The examiner can normally be reached on M-Th, 6:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on (703) 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

MAA  
September 8, 2003

NADINE G. NORTON  
PRIMARY EXAMINER  


Application/Control Number: 09/926,202  
Art Unit: 1765

Page 7